Electronic Version
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Claims

[c1] 1.A memory module comprising:
a substrate with metal contact pads along an edge of the substrate for insertion into a socket on a main board;
a plurality of memory chips mounted on the substrate;
a terminated signal line on the substrate connected to inputs on the plurality of memory chips, the terminated signal line having a driven end that is driven by a driver on the substrate or on the main board, and a far end that is farther along the terminated signal line than is the driven end;
a dynamic termination circuit attached to the far end of the terminated signal line, the dynamic termination circuit selectively connecting a low-impedance path to the far end in response to a switch signal being in an active state, but disconnecting the low-impedance path from the far end in response to the switch signal being in an inactive state;
a clock signal and a chip-select signal carried by lines on the substrate, wherein the chip-select signal is activated when the main board accesses the plurality of memory chips and wherein the plurality of memory chips operate synchronously to the clock signal when the chip-select

signal is activated; and

a switch-signal generator, mounted on the substrate, receiving the chip-select signal and the clock signal, the switch-signal generator generating the switch signal in the active state synchronously to the clock signal when the chip-select signal is activated to select the plurality of memory chips for access by the main board,

whereby the low-impedance path terminates the terminated signal line in response to the switch signal.

[c2] 2.The memory module of claim 1 wherein the low-impedance path comprises:

a low-impedance resistor; and

a switching transistor having a channel in series with the low-impedance resistor and a gate receiving the switch signal.

[c3] 3.The memory module of claim 2 wherein the low-impedance resistor has a first resistance that matches a line impedance of the terminated signal line to within an order of magnitude.

[c4] 4.The memory module of claim 2 wherein the low-impedance resistor has a first resistance that matches a line impedance of the terminated signal line to within 20%.

[c5] 5.The memory module of claim 2 wherein the switching transistor is an n-channel transistor.

[c6] 6.The memory module of claim 5 wherein the low-impedance path further comprises:
a p-channel transistor, having a channel in parallel with the switching transistor, the p-channel transistor having a gate receiving an inverse of the switch signal,
whereby a transmission gate enables conduction in the low-impedance path.

[c7] 7.The memory module of claim 5 wherein the low-impedance path is coupled between the far end of the terminated signal line and a fixed terminating voltage.

[c8] 8.The memory module of claim 7 wherein the fixed terminating voltage is a middle voltage between a ground and a power-supply voltage.

[c9] 9.The memory module of claim 8 wherein the fixed terminating voltage is about half of the power-supply voltage.

[c10] 10.The memory module of claim 7 wherein the fixed terminating voltage is a ground or a power-supply voltage.

[c11] 11.The memory module of claim 8 wherein the dynamic termination circuit further comprises:

a static terminating resistor coupled between the far end of the terminated signal line and the fixed terminating voltage;

wherein the static terminating resistor has a second resistance that is more than 1K ohms while the first resistance of the low-impedance resistor is less than 100 ohms.

[c12] 12.The memory module of claim 11 further comprising:

a clock line on the substrate, the clock line connected to clock inputs on the plurality of memory chips, wherein the clock line carries a memory clock signal that synchronizes operation of the plurality of memory chips;

wherein the memory clock signal is the clock signal or is synchronous to the clock signal applied to the switch-signal generator.

[c13] 13.The memory module of claim 12 further comprising:

a chip-select line on the substrate, the chip-select line connected to chip-select inputs on the plurality of memory chips, wherein the chip-select line is in a selected state when a controller on the main board accesses the plurality of memory chips on the substrate, but the chip-select line is in a de-selected state when the controller is not accessing the plurality of memory chips on the substrate;

wherein the chip-select line carries the chip-select signal

applied to the switch-signal generator or a logical equivalent.

[c14] 14.The memory module of claim 13 wherein the switch-signal generator generates a timing window that is a fraction of a clock period of the clock signal, the fraction being half or less of the clock period;
wherein the switch signal is generated in response to the timing window, wherein the switch signal is in the active state for no more than half of the clock period when the chip-select signal is activated.

[c15] 15.The memory module of claim 14 wherein the switch-signal generator combines the clock signal and a delayed clock signal to generate the timing window which is combined with the chip-select signal to generate the switch signal.

[c16] 16.The memory module of claim 15 wherein the delayed clock signal is delayed by about one-quarter of the clock period;
wherein the timing window is about one-quarter of the clock period;
wherein the switch signal is activated for no more than one-quarter of the clock period;
wherein power consumption by the dynamic termination circuit is reduced by at least 75% compared to an al-

ways-on termination.

[c17] 17.The memory module of claim 16 wherein the terminated signal line is formed by one or more metal traces connected together, the one or more metal traces being formed on a surface of the substrate or on a layer within the substrate.

[c18] 18.The memory module of claim 17 wherein the terminated signal line has a trunk segment, a first branch segment, and a second branch segment;
wherein the first branch segment connects to a first subset of the plurality of memory chips and to the dynamic termination circuit;
wherein the second branch segment connects to a second subset of the plurality of memory chips and to a second dynamic termination circuit that connects to a second far end of the second branch segment;
wherein the second dynamic termination circuit is a copy of the dynamic termination circuit;
whereby the terminated signal line is terminated at two far ends by dynamic termination circuits.

[c19] 19.The memory module of claim 18 wherein the trunk segment connects a junction of the first and second branch segments to the driven end of the terminated signal line;

wherein an impedance of the trunk segment is about equal to a sum of impedances of the first and second branch segments,
whereby segments of the terminated signal line are trace-impedance-matched at the junction.

[c20] 20.The memory module of claim 19 wherein the trunk segment comprises a metal trace having a double width;
wherein the first branch segment comprises a metal trace having a single width;
wherein the second branch segment comprises a metal trace having the single width;
wherein the double width is about twice the single width.

[c21] 21.The memory module of claim 20 further comprising:
a driver on the substrate that drives the driven end of the terminated signal line when the chip-select signal is activated, but not driving the terminated signal line when the chip-select is not activated.

[c22] 22.The memory module of claim 1 wherein the plurality of memory chips comprise a plurality of synchronous dynamic-random-access memory (DRAM) chips.

[c23] 23.A memory module with low-power termination comprising:
a printed-circuit board (PCB) substrate having wiring

traces formed thereon;
a clock line on the substrate for carrying a clock signal;
a chip-select line on the substrate for carrying a chip-select signal;
a plurality of synchronous memory chips, each having a clock input receiving the clock signal from the clock line and a chip-select input receiving the chip-select signal from the chip-select line and each receiving a plurality of signal inputs;
a plurality of signal lines on the substrate to the signal inputs of the plurality of synchronous memory chips, each signal line having a driven end and one or more far end;
a plurality of active terminators, each connected between a far end of one of the plurality of signal lines and a terminating voltage, the plurality of active terminators each receiving a switch signal;
wherein each active terminator in the plurality of active terminators comprises:
a static terminating resistor connected between the far end and the terminating voltage and having a resistance of 1K ohm or more;
a dynamic terminating resistor and a switch connected together in series between the far end and the terminating voltage;
wherein the dynamic terminating resistor has a resis-

tance of less than 100 ohms and selected to approximately match an impedance of a signal line connected to the far end;

wherein the switch comprises an n-channel transistor with a gate receiving the switch signal or an inverse of the switch signal, wherein the n-channel transistor conducts current through the dynamic terminating resistor when the switch signal is activated, but prevents current flow through the dynamic terminating resistor when the switch signal is not activated; and

switch timing logic, receiving the chip-select signal and the clock signal, for pulsing activate the switch signal when the chip-select signal selects the plurality of synchronous memory chips for access during a portion of a period of the clock signal.

[c24] 24.The memory module with low-power termination of claim 23 wherein the switch further comprises:

a p-channel transistor in parallel with the n-channel transistor, having a gate receiving an inverse of the switch signal when the n-channel transistor has a gate receiving the switch signal, or having the gate receiving the switch signal when the n-channel transistor has a gate receiving the inverse of the switch signal,

whereby a transmission gate enables current through the dynamic terminating resistor.

[c25] 25.An actively-terminated memory module comprising:
substrate means, with metal contact pads along an edge of the substrate means, for insertion into a socket on a main board;
a plurality of memory chips mounted on the substrate means;
terminated signal line means, on the substrate means and connected to inputs on the plurality of memory chips, for conducting a signal from a driven end to a far end, the driven end being driven by a driver on the substrate means or on the main board, and the far end being farther along the terminated signal line means than is the driven end;
high-current resistor means for terminating the terminated signal line means with a low impedance;
switch means for selectively connecting the high-current resistor means to the far end in response to a switch signal being in an active state, but for disconnecting the high-current resistor means from the far end in response to the switch signal being in an inactive state;
a clock signal and a chip-select signal carried by lines on the substrate means, wherein the chip-select signal is activated when the main board accesses the plurality of memory chips and wherein the plurality of memory chips operate synchronously to the clock signal when the chip-

select signal is activated; and

switch-signal generator means, mounted on the substrate means, receiving the chip-select signal and the clock signal, the switch-signal generator means generating the switch signal in the active state synchronously to the clock signal when the chip-select signal is activated to select the plurality of memory chips for access by the main board,

whereby the high-current resistor means terminates the terminated signal line means in response to the switch signal.